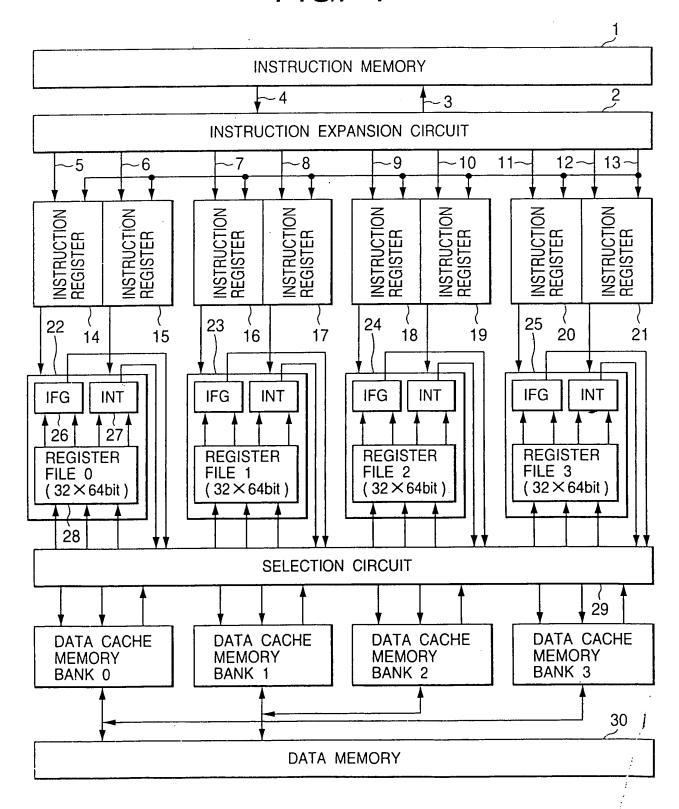
FIG. 1



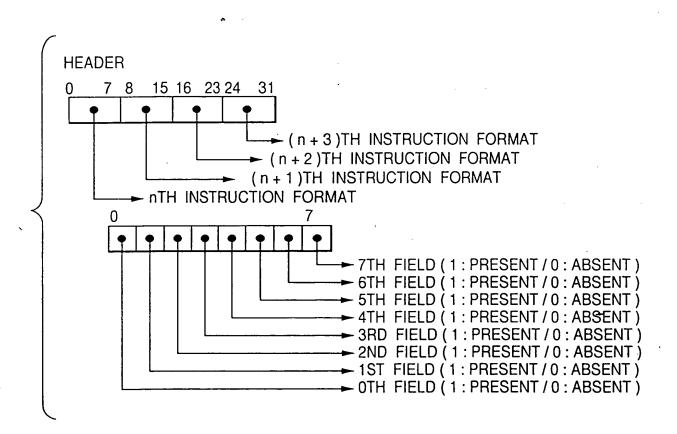
2/30 FIG. 2 SOURCE 1 S MODE SPARE SOURCE 0 (a) IFG FIELD 16 17 \ 21 22 28 (31 26 11 12 SIMD / DEST. BANK | DESTINATION OPE. CODE IMMEDIATE 0 => NORMAL MODE 0 = > CONTENT OF THE SOURCE 1 1 => SIMD MODE IS A REGISTER NO. 1 = > CONTENT OF THE SOURCE 1 IS AN IMMEDIATE VALUE IMMEDIATE VALUE (0~31) (WHEN IMMEDIATE = 1) REGISTER NO. (0 ~ 31) **DESIGNATION OF** (WHEN IMMEDIATE = 0) OPERATIONS (256 KINDS MAX.) DEST. BANK (WHEN S MODE = 0) SAME WITH INT FIELD SIMD (WHEN S MODE = 1)DESIGNATE AN INSTRUCTION EXECUTED BY THREE OTHER BANKS 0 = > NOP1 => EXECUTE THE SAME INSTRUCTION CORRESPONDENCE BETWEEN THE BIT POSITION AND THE BANK CHANGES IN ACCORDANCE WITH THE INSTRUCTION REGISTER, AS SHOWN IN THE TABLE BELOW REGISTER CORRESPONDENCE BETWEEN SIMD POSITION OF NO. BIT POSITION AND THE BANK # THE INSTRUCTION |  $(0 \sim 31)$ REGISTER 10 11 INSTRUCTION BANK 2 BANK 3 BANK 1 REGISTER 14 INSTRUCTION BANK 3 BANK 2 BANK 0 REGISTER 16 INSTRUCTION BANK 1 BANK 3 BANK 0 **REGISTER 18** INSTRUCTION BANK 1 BANK 2 BANK 0 **REGISTER 20 BRANCH TEST DEST. BANK** 18 19 23 24 31 13 14 11 10 DESTINATION SOURCE 1 OPE, CODE IMMEDIATE (b) INT FIELD SOURCE 0 000 = > BANK 0000 = > FAULSE001 = > BANK 1 001 => TRUE IMMEDIATE VALUE (0 ~ 255) 010 = > BANK 2010 = > BRANCH BANK REGISTER 2 (WHEN IMMEDIATE = 1) 011 = > BANK 3011 => BRANCH BANK REGISTER 3 REGISTER NO. (0~31) 100 = > BANK 4 100 = > BRANCH BANK REGISTER 4 (WHEN IMMEDIATE = 0) 101 = > BANK 5 101 => BRANCH BANK REGISTER 5 110 = > BANK 6110 => BRANCH BANK REGISTER 6

111 => BANK 7

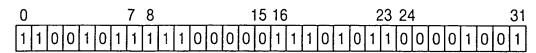
111 => BRANCH BANK REGISTER 7

AN EXAMPLE OF A PROGRAM STORAGE INTO THE INSTRUCTION MEMORY 31 0 HEADER 0 FIELD 0 FIELD 6 FIELD 7 FIELD 0 FIELD 1 FIELD 1 FIELD 4 63 32 FIELD 2 FIELD 4 FIELD 6 FIELD 7 FIELD 4 FIELD 2 FIELD 0 FIELD 1 95 67 64 FIELD 7 FIELD 0 FIELD 2 FIELD 3 FIELD 6 FIELD 4 **HEADER 1** FIELD 1 1ST INSTRUCTION (ADDRESS NOS. 4~23) 2ND INSTRUCTION (ADDRESS NOS. 24~35) 3RD INSTRUCTION (ADDRESS NOS. 35 ~ 59) 4TH INSTRUCTION (ADDRESS NOS. 60 ~ 67) 5TH INSTRUCTION (ADDRESS NOS. 72 ~ 79) 6TH INSTRUCTION (ADDRESS NOS. 80 ~ 87) 7TH INSTRUCTION (ADDRESS NOS. 88~91) 8TH INSTRUCTION (ADDRESS NOS. 92 ~ 95)

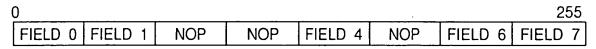
FIG. 4



HEADER 0



1 (n)TH INSTRUCTION FORMAT



2 (n+1)TH INSTRUCTION FORMAT

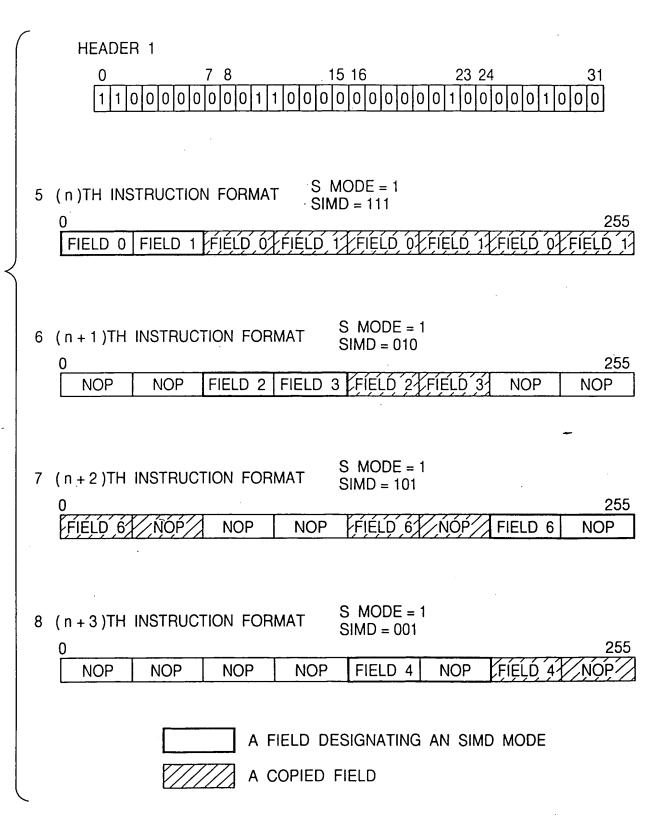
0							<del>-</del> 255
FIELD 0	FIELD 1	FIELD 2	NOP	NOP	NOP	NOP	NOP

3 (n+2)TH INSTRUCTION FORMAT

0							255
FIELD 0	FIELD 1	FIELD 2	NOP	FIELD 4	NOP	FIELD 6	FIELD 7

4 (n+3)TH INSTRUCTION FORMAT

0			_					255
	NOP	NOP	NOP	NOP	FIELD 4	NOP	NOP	FIELD 7



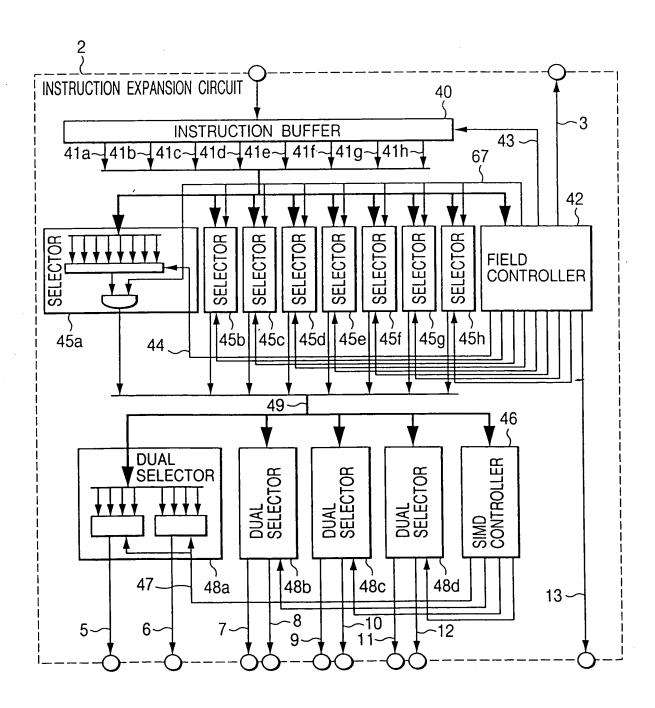
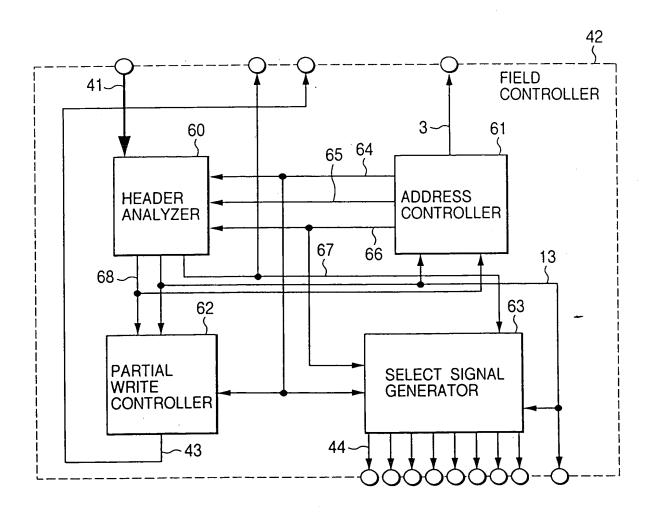


FIG. 8



AN EXAM	PLE OF	- A	PROGRA	M STO	RA	GE INT	0	THE IN	IST	RUCTION	٧	мемо	RY
0													31
HEADER	FIELD	0	FIELD 1	FIELD	4	FIELD	6	FIELD	7	FIELD C	) [	FIELD	1
32													63
FIELD 2	FIELD	0	FIELD 1	FIELD	2	FIELD	3	FIELD	4	FIELD 5		FIELD	6
64			72									_	95
FIELD 7	FIELD	0	HEADER	FIELD	0	FIELD	1	FIELD	2	FIELD 3	3 [	FIELD	4
96				108								1	127
FIELD 5	FIELD	6	FIELD 7	FIELD	1	FIELD	2	FIELD	3	FIELD 0		FIELD	4

ТО	T1	T2	T3	. T4	T5	T6	T7	T8
IF	EXP	EXE	WB	INSTRUCT	TON 1			
	IF	EXP	EXE	WB	INSTRUCT	TON 2		
INSTR	UCTION 3	IF	EXP	EXE	WB			
	INSTR	UCTION 4	IF	EXP	EXE	WB		
		INSTR	UCTION 5	IF	EXP	//EXP2/	EXE	WB
				INSTR	UCTION 6	IF	EXP	EXE
REFETCH 0	SIGNAL 0	LINE 13 0	0	0	0		0	0
0	TION LEN	12	32	8 4	36		12	8
INSTRUC 0	TION ADD 0	RESS BUS 24	36 36	68	72	//108///	108	120
ADDRESS 0	S BUS 3 32	56	68	100	104	///136///	140	152
WRITE E	NABLE BU 11111100	IS 43 10000011	11111111	01000000	111111111	00100000	00011100	00000011
DATA LA	TCHED IN	THE INS	TRUCTION	BUFFER4	0			
HEADER 0	ADDRESS 0	BUS 65	2	3	0		1	2
	( SELECT	SIGNAL 44   6	)	1	3		-	6
FIELD 1	2	7	2	-	4	V/// <u>-</u> ///	3	
FIELD 2		0	3	-	5	<i>\\\\;\\\\</i>	4	<u> </u>
FIELD 3	-	•	4	-	6	<i>\\\;</i>	5	
FIELD 4	3	•	5	<u> </u>	7		<del>] -</del>	7
FIELD 5		-	6	<u> </u>	0	<i>\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\</i>	<del>]</del>	-
FIELD 6	<del></del>	<u> </u>	7		1	Y//ii///	1	-
FIELD 7	5		0	•	•	2	<u> </u>	

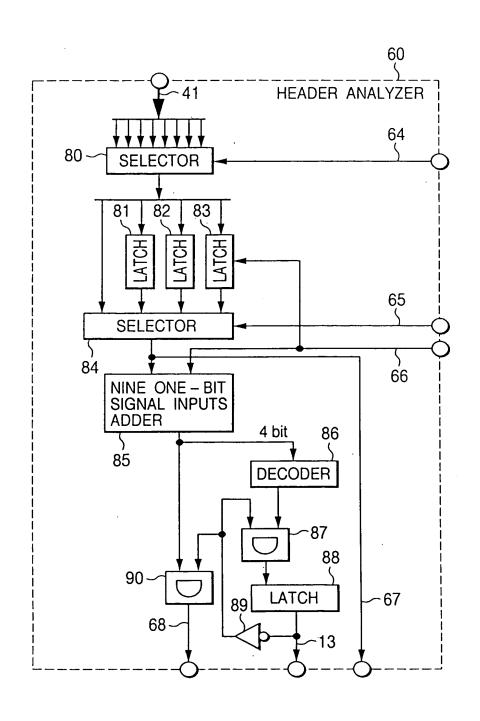


FIG. 12

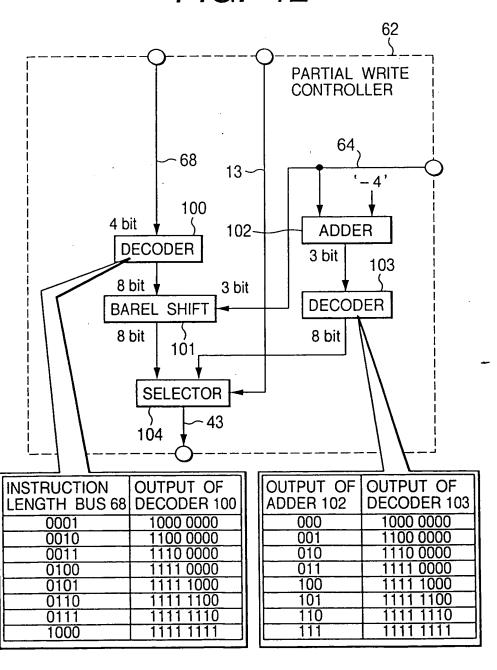
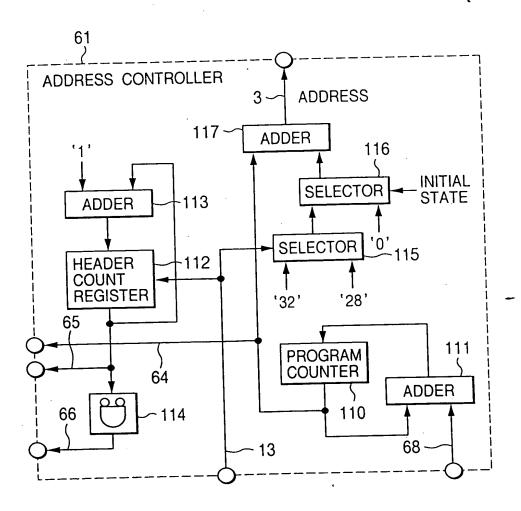
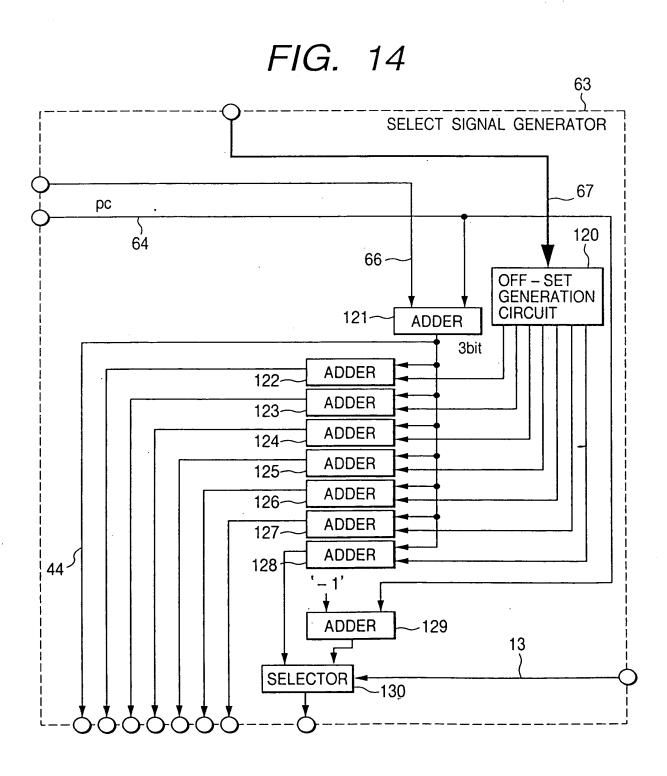


FIG. 13







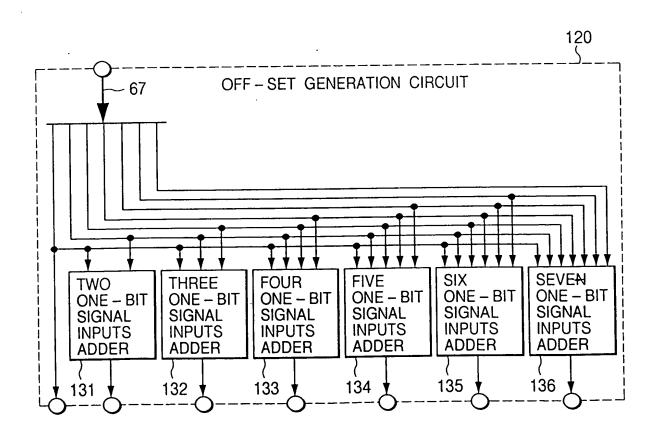


FIG. 16

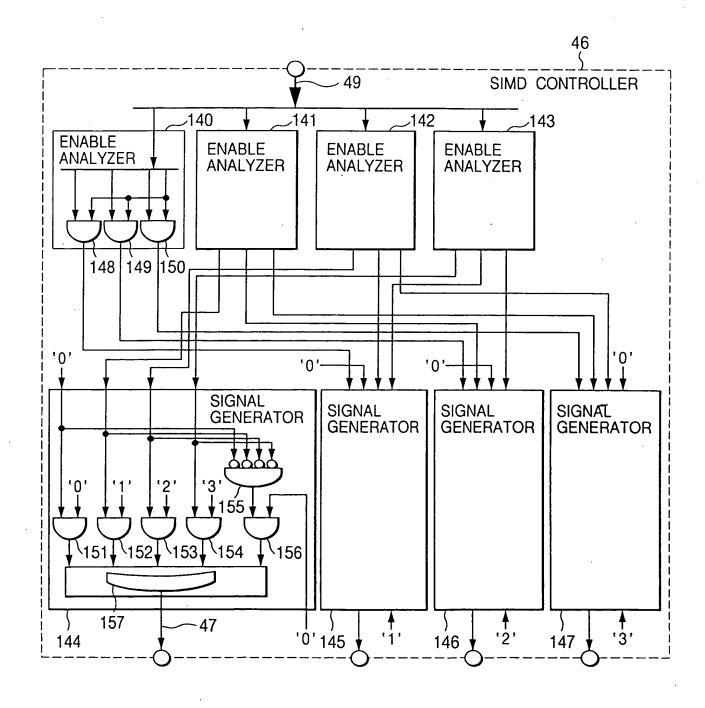
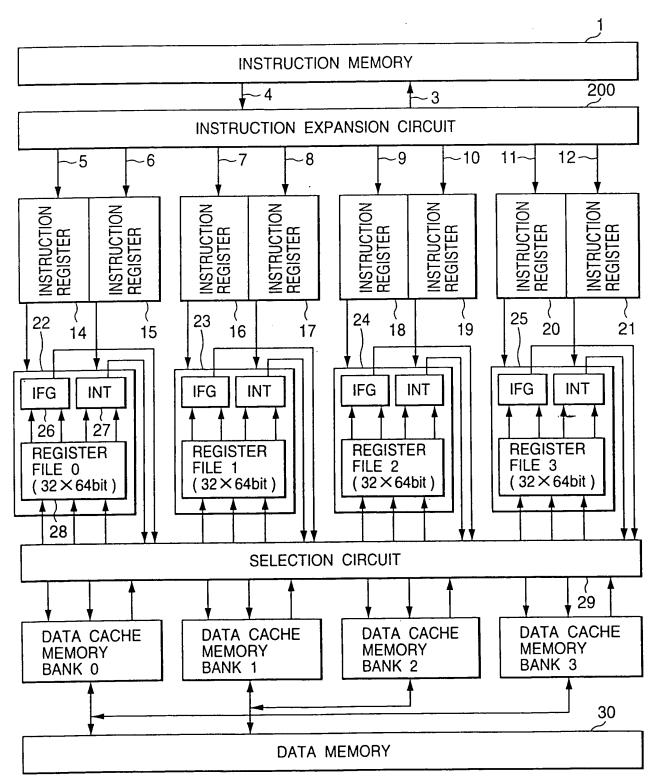


FIG. 17



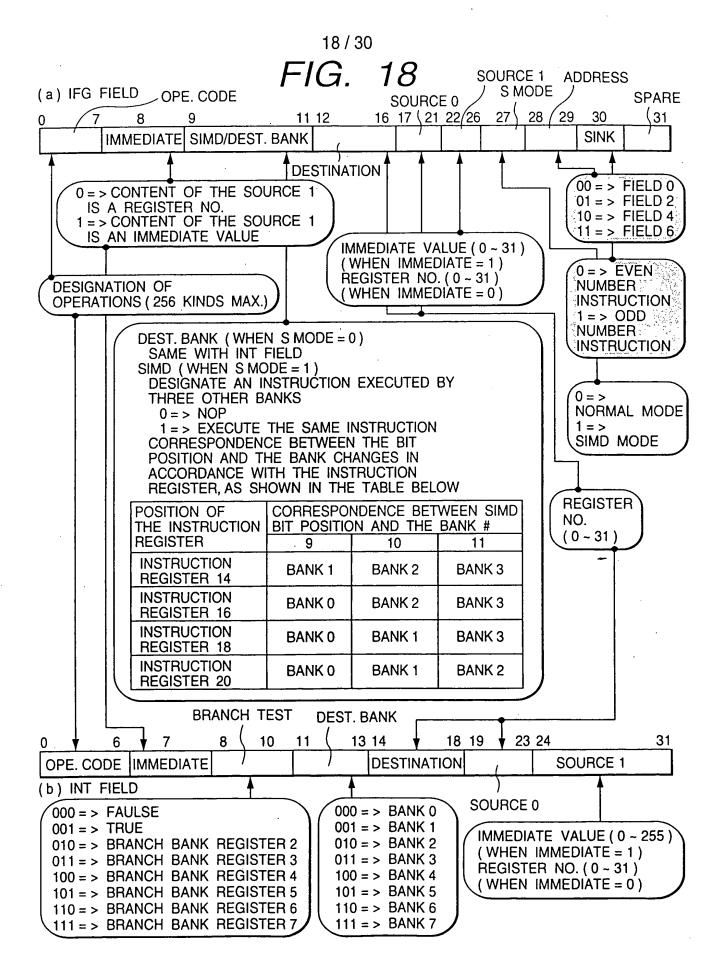


FIG. 19

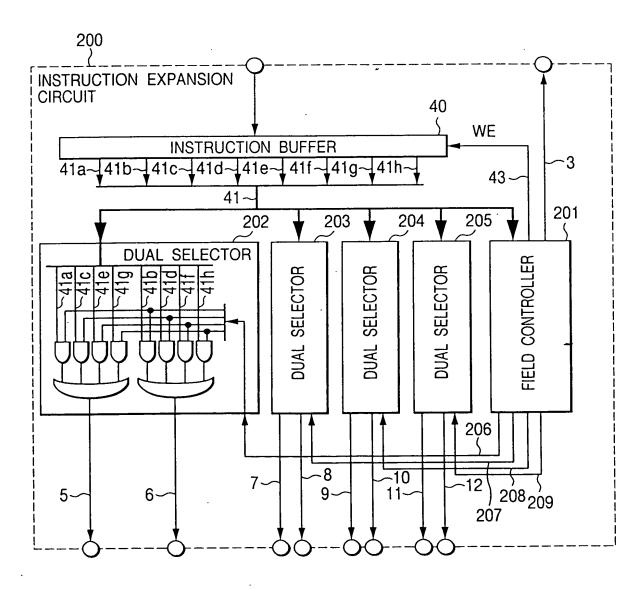
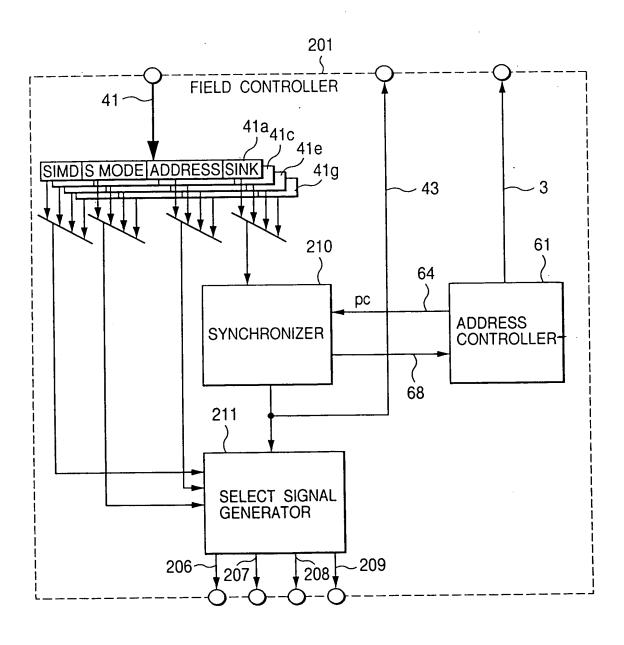


FIG. 20



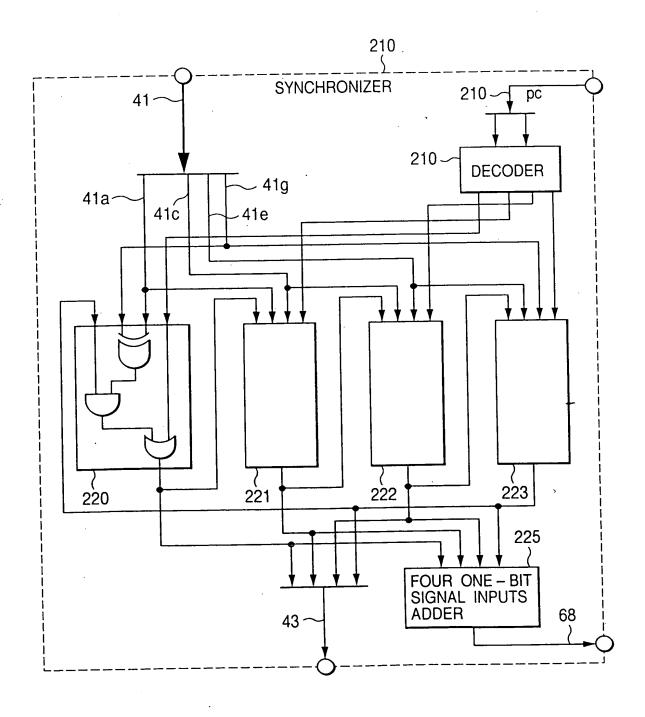


FIG. 22

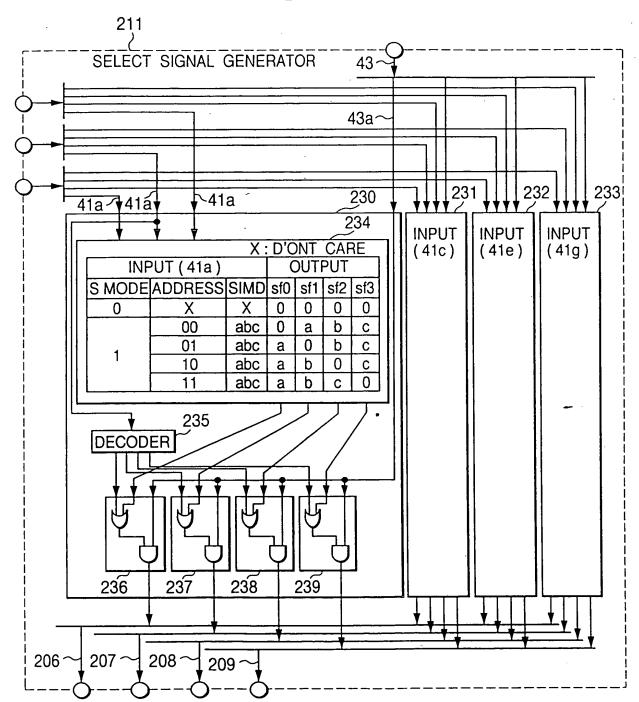
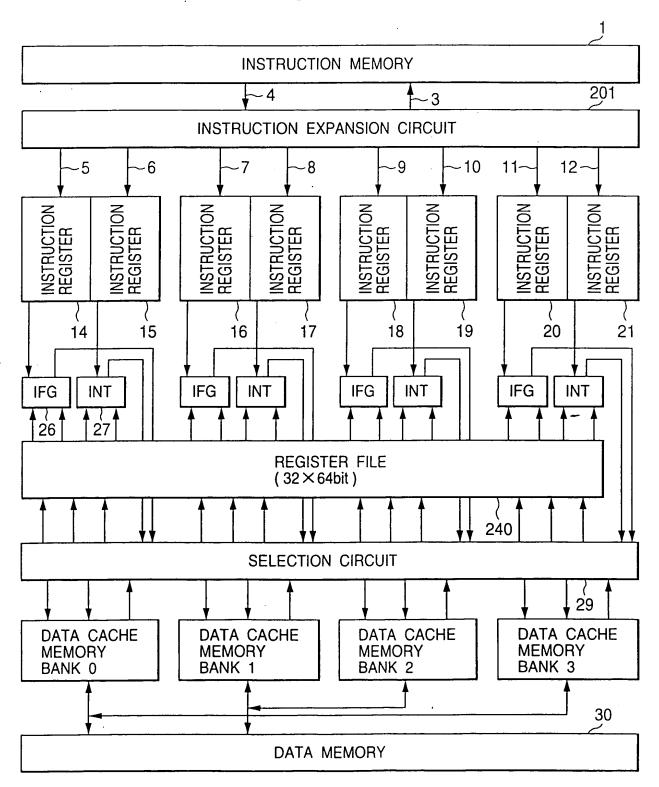
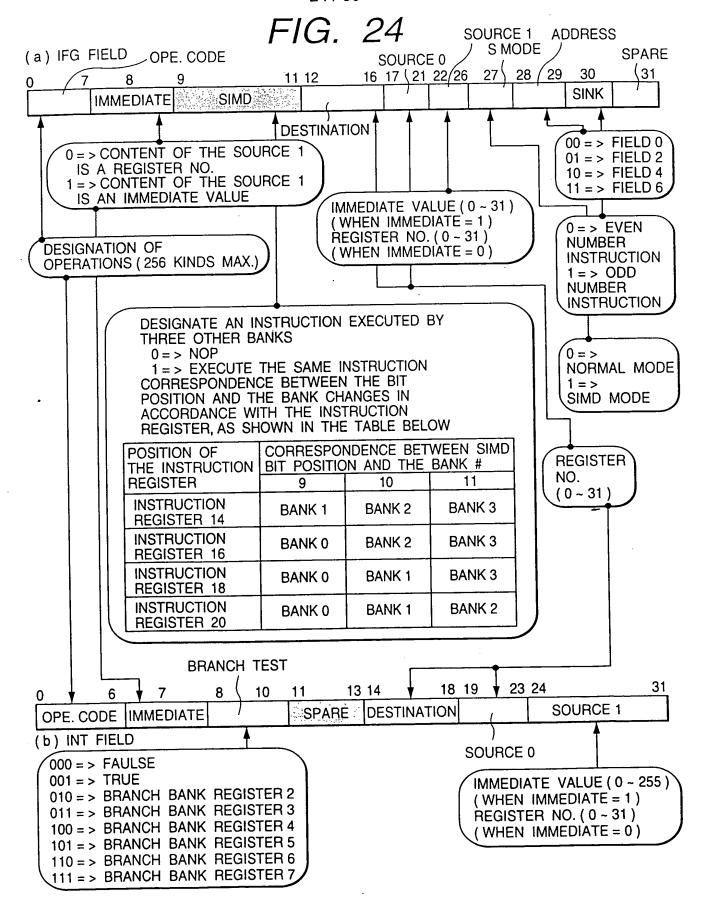
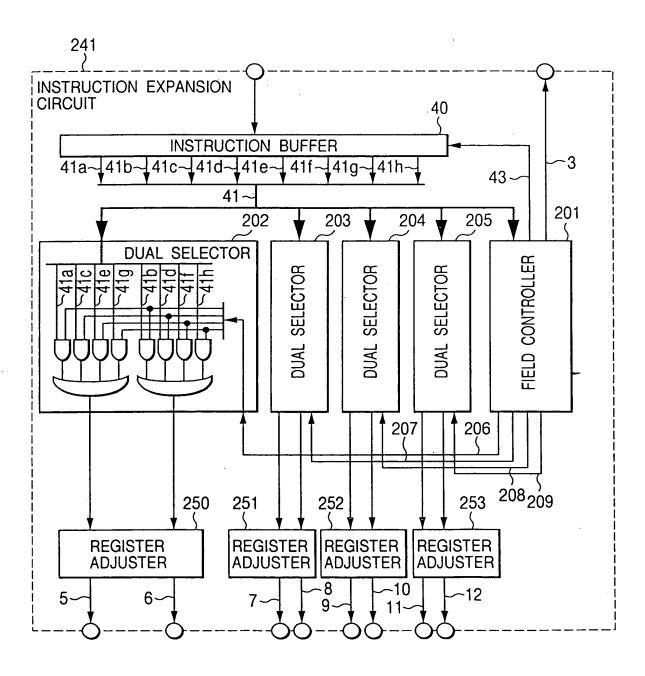


FIG. 23



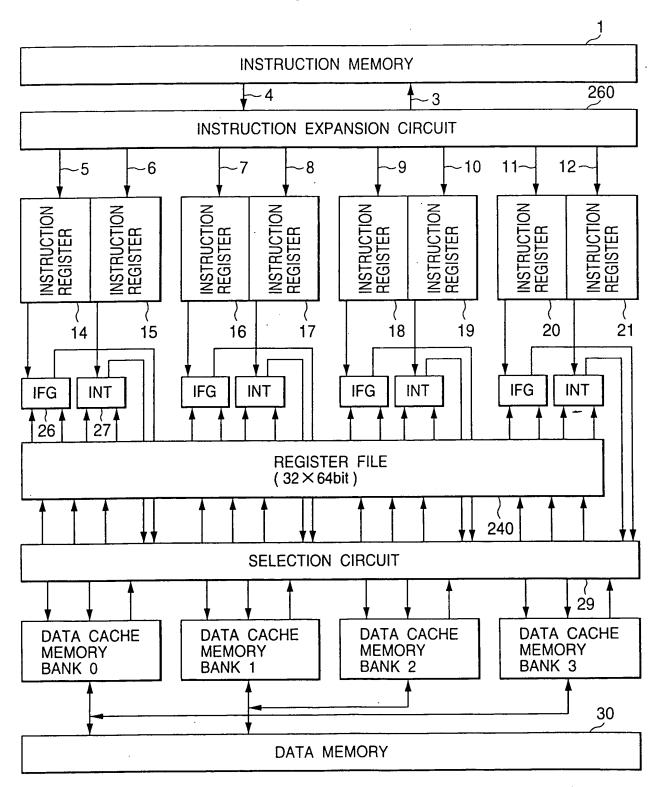
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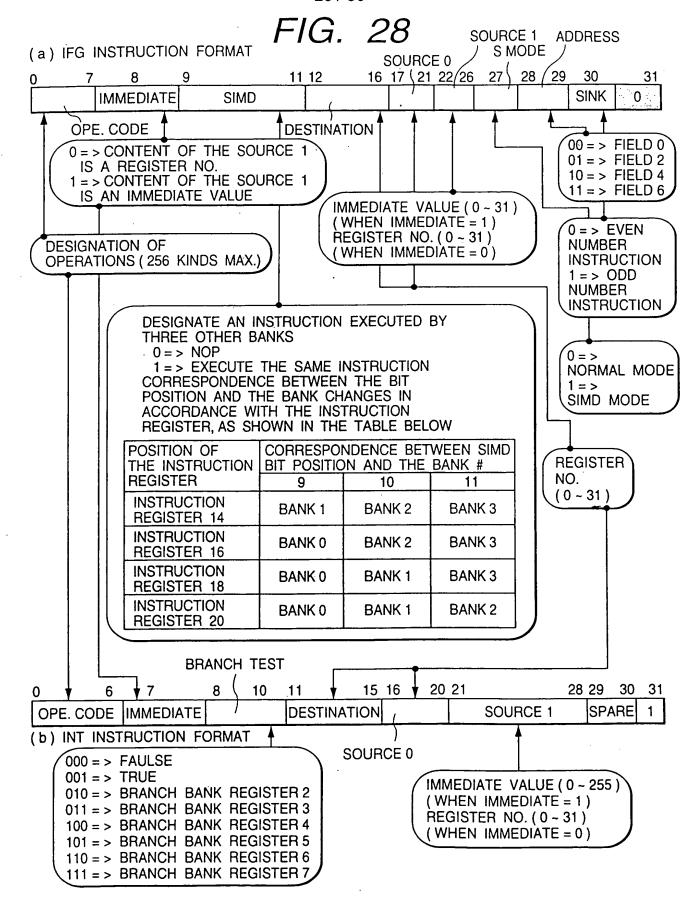


I	NPUT FIEL	OUTPUT FIELD	
SMODE	<b>ADDRESS</b>	REGISTER#	REGISTER#
0	X	N	N
	00	N	N
	01	N	N + 3
1	10	N	N + 2
	11	N	N + 1

FIG. 27



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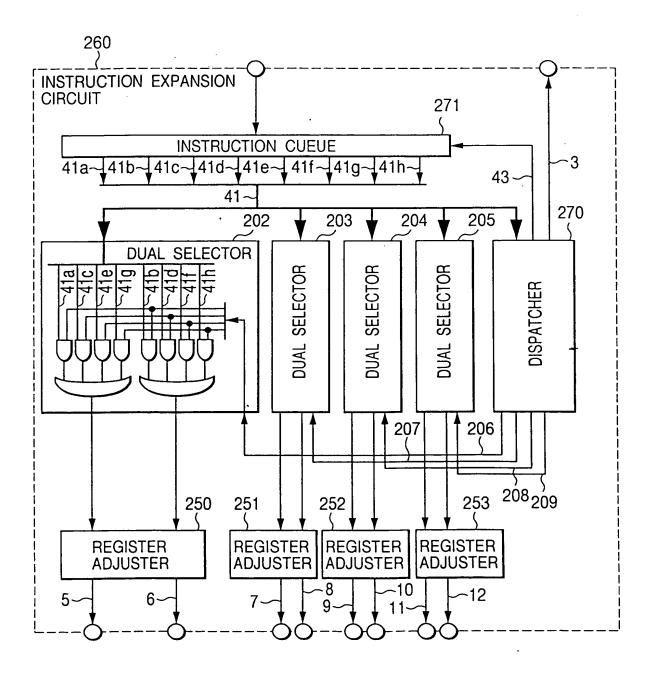


FIG. 30

